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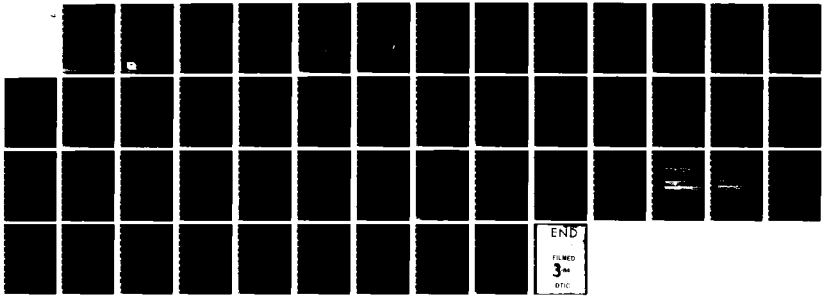

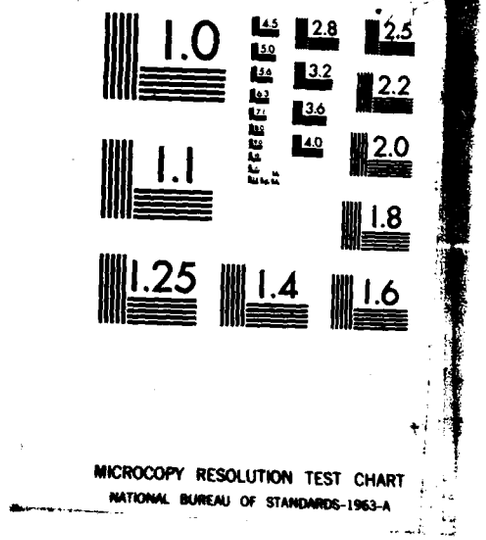
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VHSIC TECHNOLOGY WORKING GROUP REPORT

(IDA/OSD R&M STUDY)

Egbert Maynard
OUSDRE
Working Group Chairman

November 1983

Prepared for

Office of the Under Secretary of Defense for Research and Engineering
and
Office of the Assistant Secretary of Defense
(Manpower, Reserve Affairs and Logistics)

INSTITUTE FOR DEFENSE ANALYSES
SCIENCE AND TECHNOLOGY DIVISION

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This document records the activities and presents the findings of the VHSIC Technology Working Group part of the IDA/OSD Reliability and Maintainability Study, conducted during the period from July 1982 through August 1983.

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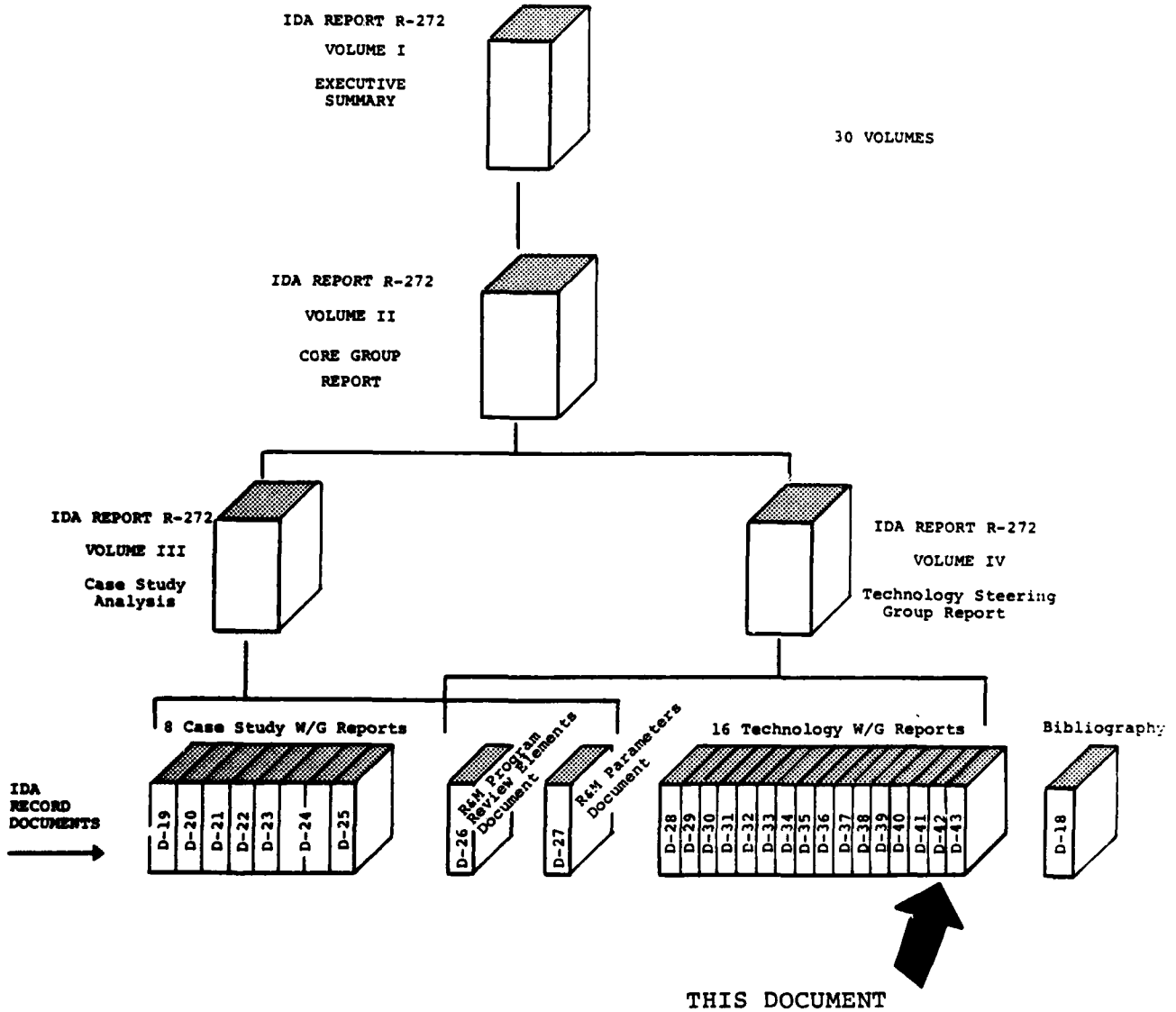
SCIENCE AND TECHNOLOGY DIVISION
1801 N. Beauregard Street, Alexandria, Virginia 22311

Contract MDA 903 79 C 0018
Task T-2-126

RELIABILITY AND MAINTAINABILITY STUDY

— REPORT STRUCTURE —



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PREFACE

As a result of the 1981 Defense Science Board Summer Study on Operational Readiness, Task Order T-2-126 was generated to look at potential steps toward improving the Material Readiness Posture of DoD (Short Title: R&M Study). This task order was structured to address the improvement of R&M and readiness through innovative program structuring and applications of new and advancing technology. Volume I summarizes the total study activity. Volume II integrates analysis relative to Volume III, program structuring aspects, and Volume IV, new and advancing technology aspects.

The objective of this study as defined by the task order is:

> "Identify and provide support for high payoff actions which the DoD can take to improve the military system design, development and support process so as to provide quantum improvement in R&M and readiness through innovative uses of advancing technology and program structure."

The scope of this study as defined by the task order is:

> To (1) identify high-payoff areas where the DoD could improve current system design, development program structure and system support policies, with the objective of enhancing peacetime availability of major weapons systems and the potential to make a rapid transition to high wartime activity rates, to sustain such rates and to do so with the most economical use of scarce resources possible, (2) assess the impact of advancing technology on the recommended approaches and guidelines, and (3) evaluate the potential and recommend strategies that might result in quantum increases in R&M or readiness through innovative uses of advancing technology.

The approach taken for the study was focused on producing meaningful implementable recommendations substantiated by quantitative data with implementation plans and vehicles to be provided where practical. To accomplish this, emphasis was placed upon the elucidation and integration of the expert knowledge and experience of engineers, developers, managers, testers and users involved with the complete acquisition cycle of weapons systems programs as well as upon supporting analysis. A search was conducted through major industrial companies, a director was selected and the following general plan was adopted.

General Study Plan

Vol. III	• Select, analyze and review existing successful program
Vol. IV	• Analyze and review related new and advanced technology
Vol. II	(• Analyze and integrate review results (• Develop, coordinate and refine new concepts
Vol. I	• Present new concepts to DoD with implementation plan and recommendations for application.

The approach to implementing the plan was based on an executive council core group for organization, analysis, integration and continuity; making extensive use of working groups, heavy military and industry involvement and participation, and coordination and refinement through joint industry/service analysis and review. Overall study organization is shown in Fig. P-1.

The basic technology study approach was to build a foundation for analysis and to analyze areas of technology to surface: technology available today which might be applied more broadly; technology which requires demonstration to finalize and reduce risk; and technology which requires action today to provide reliable and maintainable systems in the future. Program structuring implications were also considered. Tools used to accomplish

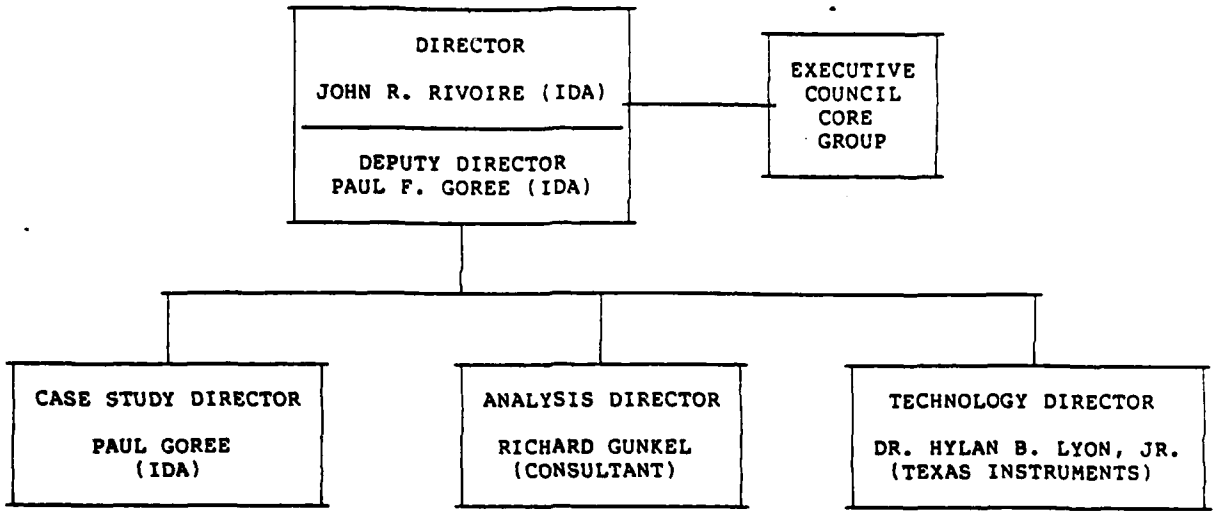

FIGURE P-1. Study Organization

this were existing documents, reports and study efforts such as the Militarily Critical Technologies List. To accomplish the technology studies, sixteen working groups were formed and the organization shown in Fig. P-2 was established.

This document records the activities and findings of the Technology Working Group for the specific technology as indicated in Fig. P-2. The views expressed within this document are those of the working group only. Publication of this document does not indicate endorsement by IDA, its staff, or its sponsoring agencies.

Without the detailed efforts, energies, patience and candidness of those intimately involved in the technologies studied, this technology study effort would not have been possible within the time and resources available.

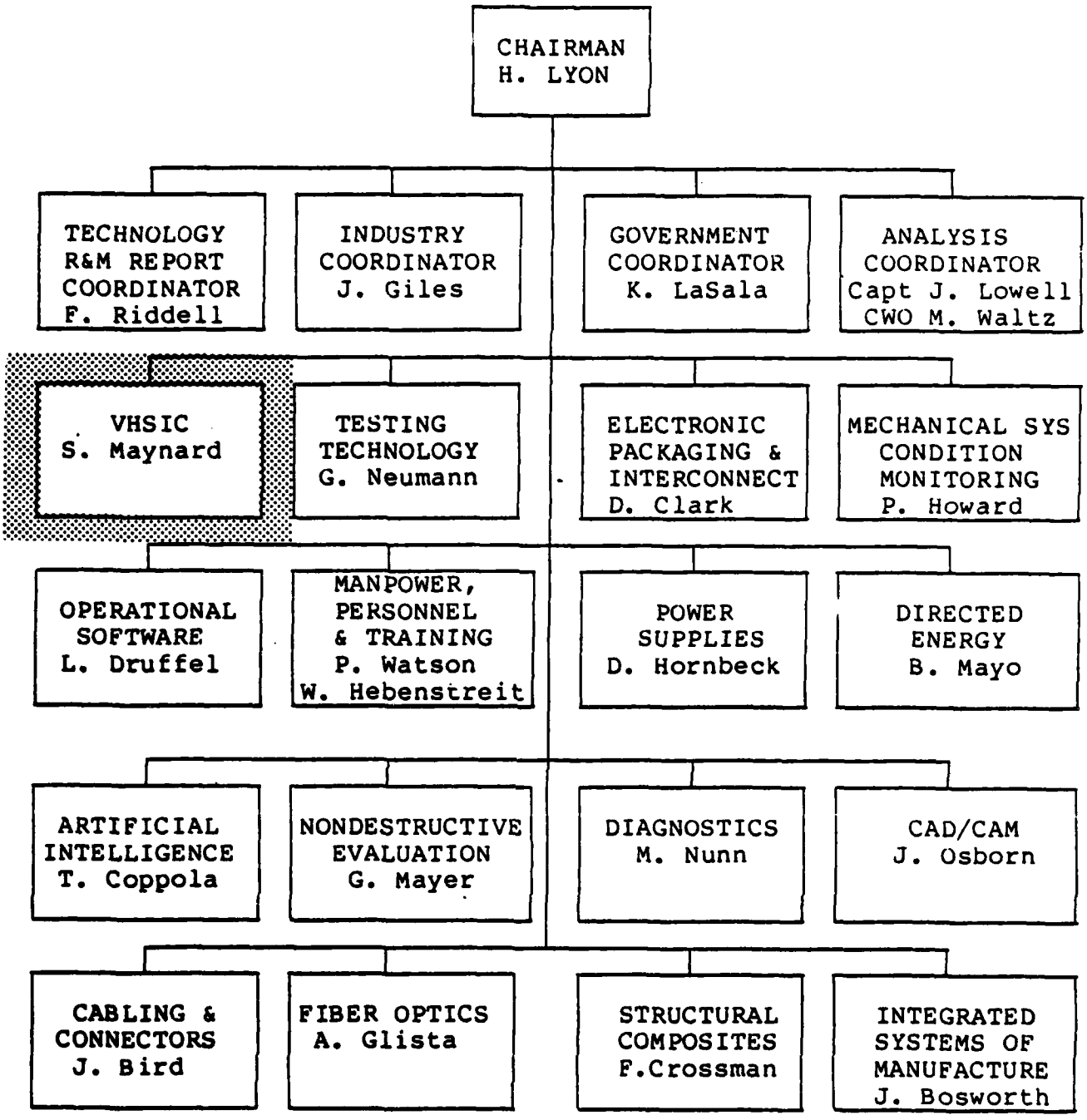

FIGURE P-2. Technology Study Organization

OSD/IDA R & M STUDY

VHSIC TECHNOLOGY WORKING GROUP

REPORT

Submitted by

Egbert Maynard
OUSDR&E, Director
VHSIC/Electronics Devices

NOVEMBER 1983

ACKNOWLEDGEMENT

The VHSIC Technology Working Group is indebted to Deborah Franke and Thomas Mitchell, of Digital Systems Research, Systems and Measurements Division, Research Triangle Institute, for their valuable assistance in providing Chapter II of this report.

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I VHSIC

A INTRODUCTION

As were all the technology working groups, the VHSIC study activities were guided by the overall study objectives as stated in the Task Order, namely:

> "To identify and provide support for high-payoff actions which the DoD can take to improve the military system design, development and support process so as to provide quantum improvements in R&M and readiness through innovative uses of advancing technology and program structure. The DoD objective is to enhance the peacetime availability of major weapons systems and to enhance the ability to make a rapid transition to high wartime activity rates, to sustain such rates and to do so with the most economical use of scarce resources possible."

To address these objectives, this report is divided into three sections. The first of these sections describes, in summary, the VHSIC Program. Included in this summary is a Program "Road Map" (Fig. 1) and the identification of several key program elements which are planned or in place to support many of the above stated objectives. The second section of this report addresses, in particular, the reliability/availability question. The final section contains a summary and recommendations for further efforts relative to utilizing the potential of VHSIC in the R&M arena.

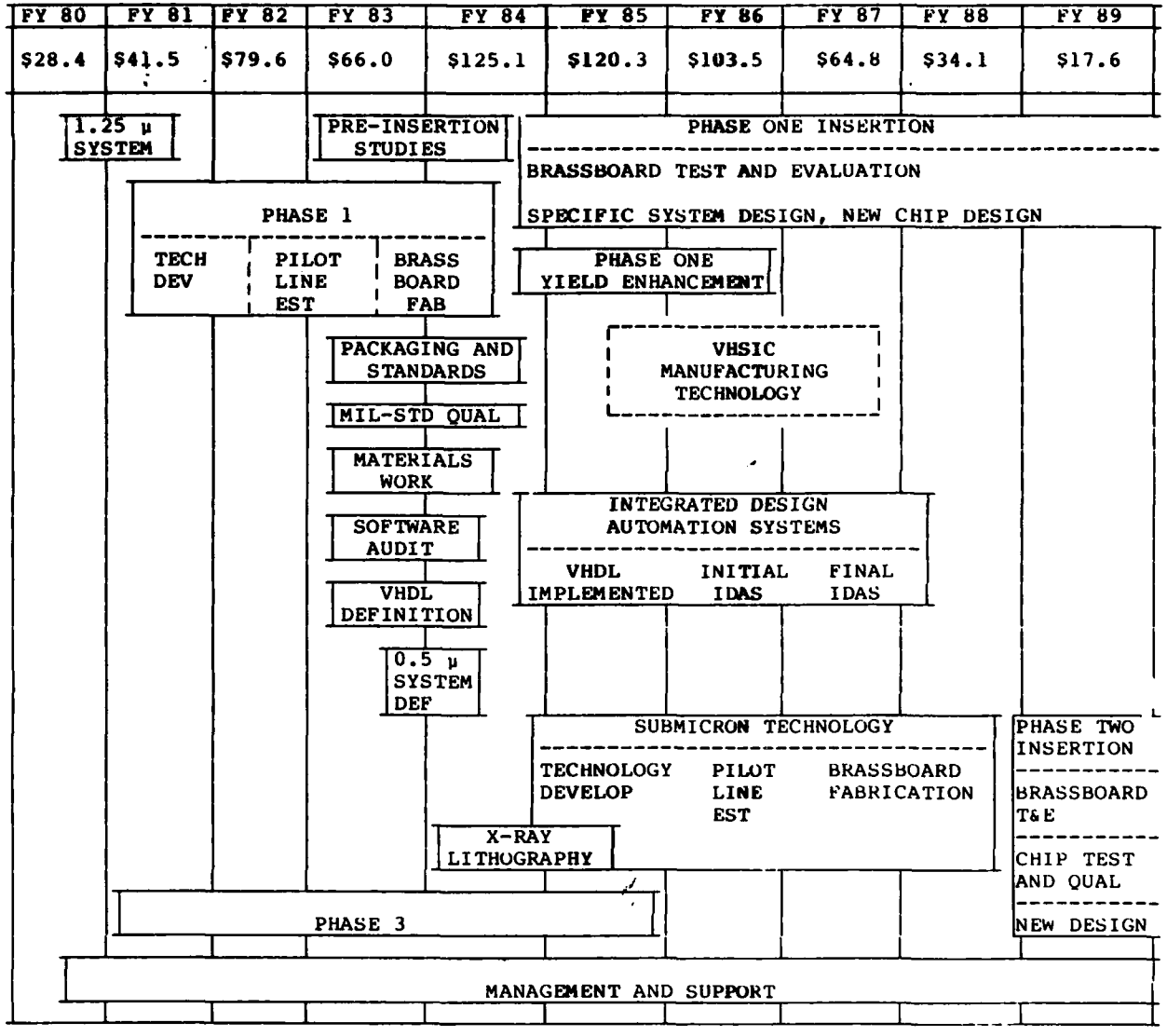

FIGURE 1. VHSIC Program Road Map

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B VERY HIGH SPEED INTEGRATED CIRCUITS (VHSIC) PROGRAM SUMMARY

The VHSIC Program is a tri-Service program with the goal of developing and inserting advanced very large scale integrated circuits into operational military systems. VHSIC devices will have a functional throughput of approximately 100 times greater than commercially available integrated circuits. These devices will be hardened to current tactical environments, include build-in-test, and result in better reliability and lower cost for military systems. The twenty-nine VHSIC chips and the six demonstration brassboards currently being developed are structured toward meeting military requirements in real time signal processing for such areas as acoustic signal processing, radar signal processing, electro-optics signal processing, electronic warfare signal processing, anti-jam communications, and multimode fire-and-forget missiles.

The major elements of the program and their time schedules are shown below and in the attached chart (VHSIC Program Road Map):

- Phase 0, was begun in March 1980 to define the specific tasks necessary to meet the program goals for the 1.25 micrometer technology.

  $ 10.5M

- Phase 1, was begun in May 1981 with six prime contractors and the goal of developing pilot production lines for silicon chips with 1.25 micrometer feature sizes, and associated brassboards by mid-1984. Funding was increased to cover six contracts instead of two or three.

  167.8M

- Phase 2, is scheduled to start in 1984 for the development of pilot production lines and brassboards using silicon chips with 0.5 micrometer feature sizes.

  83.6M

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- Phase 3, was begun in 1980 to run in parallel with phases 1 and 2. The effort consisted of 59 contracts to industry and universities for effort in various technical problems.

  36.8M

- Management and Support, was begun in 1980 to provide for the administrative and technical support required for management of the program over ten year period.

  40.0M

The above five items constitute the original VHSIC program, proposed at a level of $223.4M but expanded to $338.7M in order to broaden contractor participation in Phase 1 and to require second sourcing for all VHSIC chips.

The following additional efforts have been added to the total scope of the program:

- Phase 3, additional efforts were started in FY83 with FY82 monies reprogrammed by HASC for work required in materials, technology insertion studies, 0.5 micrometer system definition and design software.

  14.1M

- Technology Insertion, was begun in FY83 with pre-insertion studies from Phase 3, and is funded in FY84 to begin specific system/chip designs for utilization of Phase 1 (1.25 micrometer) technology. The insertion program will require and includes the development of an integrated design automation system.

  211.8M

- Yield Enhancement, will begin in FY84 to increase the output yield of the Phase 1 pilot lines in order to make VHSIC available and affordable for the Technology Insertion programs and for expected follow-on production needs.

  90.0M

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- Phase 2, brassboard demonstrations have been added to the original submicron technology development effort. 25.5M

Total program cost.....$680.1M

The program management is based on a tri-Service/DoD effort. The overall Program Director is in the Office of the Undersecretary of Defense for Research and Engineering. He is teamed with Program Directors from each of the three Services for coordination of technical, financial, and policy matters and frequent periodic program reviews. The day-to-day technical decisions and contract administration are left to the separate services. The Defense Nuclear Agency is also on the management team and has taken an active cooperative role in VHSIC by supporting the efforts to upgrade VHSIC fabrication processes in order to meet space radiation hardness requirements.

The DoD considers that VHSIC is essential for both our near term and our long term system developments. VHSIC has a very high priority in the DoD research and development plans. Previous posture statements to the Congress have asserted that "VHSIC is our highest priority technology and we will continue to provide strong management emphasis...". It is now also receiving major additional emphasis and funding in our planned Manufacturing Technology program through FY1987. The response of the industry to the emphasis on VHSIC has been to invest corporate funds in excess of three times these amounts. VHSIC has had and will continue to have constructive interaction with both the silicon IC industry which manufactures integrated circuits and with systems contractors who will use VHSIC technology in future defense systems.

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C CURRENT PROGRAM STATUS

For over three years the pace of the VHSIC program has been very intense. During the past year, the VHSIC program has scored a number of technological successes:

- The first several Phase 1 (1.25 micron) VHSIC chips have become realities and many of the remaining chips are in the final stages of fabrication and test.
- The design and fabrication of the brassboards are well underway for demonstrating the use of the Phase 1 VHSIC chip sets in system applications.
- Vigorous efforts have started in all three services to insert VHSIC technology into a wide variety of systems.
- Solid progress has been made on the organization and use of computer aided design systems which can serve the user community in the rapid, interactive design of VHSIC complexity chips.

1. Chip and Brassboard Fabrication

This past year all of the VHSIC contractors have transitioned their paper designs and their laboratory scale fabrication procedures into designs that are being "cast in silicon" and into pilot production lines that are generating respectable process control data. Along the way some very difficult technology problems have had to be solved - such things as large area multi-level metalization, and fitting the desired chip functionality onto the finite amount of chip area available. The brassboard designs are now entering the hardware stage since accurate assessments can now be made of total chip count, input-output terminal requirements, thermal dissipation, and chip package configuration. The VHSIC program office is confident that the Phase 1 VHSIC chips and brassboards will be successfully delivered.

2. Technology Insertion/IDAS

The use of new technologies in system developments always presents the system program manager with the risk of cost escalation and schedule slips. In order to minimize these risks the VHSIC program office is providing seed money for joint funding ventures with system managers which will enable them to pursue the VHSIC technology in parallel with their more conventional approaches. Each Service has selected five systems under current development to receive VHSIC insertion funds during fiscal year 83. The following list of technology insertion candidates, under both VHSIC funding and non-VHSIC funding, includes candidates that cover almost all platforms and all the major military missions such as surveillance, communications, electronic warfare, guidance and control, and command centers.

3. VHSIC Funded:

Army
- TOW-2, missile guidance line (brassboard)
- Ground vehicle signal processor for fire control (brassboard)
- Airborne signal processor for LHX helicopter (study)
- Hellfire, Joint Services seeker (study)
- Patriot Radar, threat signal processor (study)

Navy
- AN/UYS-1, sonar signal conditioner (brassboard)
- F/A-18, airborne programmable radar signal processor (brassboard)
- AN/AYK-14, standard airborne computer (study)
- Advanced Light Weight Torpedo (study)
- Enhanced Modular Signal Processor, sonar signal processor (brassboard)

Air Force
- AN/ALQ-131, electronic warfare pod (brassboard)
- Modular Avionics Design, advanced standard modules (study)
- Launch and Leave Guided Bomb, (brassboard)
- 1750A general purpose computer, (brassboard)
- Common signal processor, (brassboard)

4. Non-VHSIC Funded:

Brassboards
- M-1 tank, imager and fire control (Army)
- Position Location and Reporting System and Joint Tactical Information Distribution System (Army)
- Remotely Piloted Vehicle, imager (Army)
- EHF SATCOM, spaceborne communications on-board processor (Navy)

Studies
- A wide variety of A/N/AF systems

It is planned to select several additional candidates from each service in FY84. Our goal for the insertion programs is to provide an early proving ground for VHSIC technology in a variety of realistic system applications which demonstrate greatly improved performance coupled with increased reliability and lower life cycle cost.

As part of the Technology Insertion program, the DoD intends to ensure that the largest number of DoD contractors possible will have access to VHSIC design technology and information at all the levels appropriate to their needs. This effort has begun with the development of a comprehensive VHSIC hardware description language (VHDL) which will allow all designers to communicate

more effectively with each other and which will be a most important tool for the smooth transfer of VHSIC technology within the defense community.

The long term approach to chip design for use in Technology Insertion is the development of a fully integrated hierarchical design system covering the levels from system partitioning to logic design and mask generation. This integrated design automation system (IDAS) will greatly reduce the time that it takes to develop and modify the design of complex chips. By making such a powerful design tool available to all qualified defense contractors and by providing a common design language, it is fully expected that the defense community will have the widest possible flexibility in using the VHSIC technology and the VHSIC design database. It is also expected that this design freedom and flexibility will encourage new system architectures and system applications which currently are not feasible nor even thought of.

5. Chip Availability and Production

To support the Technology Insertion efforts, a substantial Yield Enhancement program and a Chip Qualification program has been initiated. The first is aimed at increasing the yield of the Phase 1 pilot production lines by at least 10-fold so as to reduce the cost of the VHSIC chips and to ensure their availability to users. The Chip Qualification program will provide the system Program Manager with a measurable confidence that the VHSIC components he receives will meet his requirements.

A $90M Manufacturing Technology program that directly supports the future production of VHSIC components is now planned. This MT program will be closely coordinated in time and topic with the VHSIC Yield Enhancement program and will provide the means for translating all the VHSIC efforts into a broad, affordable, national, industrial capability.

6. Submicron

The goal of Phase 2 is to develop and demonstrate a 0.5 micrometer silicon technology which operates at a 100MHz clock rate and has a throughput of 10^{13} gate-Hz/cm^2. This advance technology goal is required in order to maintain our position of military preparedness in future weapon systems. The System Definition part of the Phase 2 submicron program has already been started. Nine contractors have been selected to study the best way to proceed with both the required submicron technology itself and with the principal system opportunities for submicron technology insertion. Three new contractors in addition to the six Phase 1 contractors have been added in this Phase - namely Harris, RCA, and Western Electric.

These studies will define the specific chips and chip sets which will be developed in Phase 2 and be used to demonstrate advanced system capabilities in such military systems as:

- "Brilliant" autonomous munitions
- Wide area ocean surveillance
- Zero "CEP" weapons
- Battlefield management
- C^3I "trusted" systems
- Artificial intelligence "engines"

7. Control of Technology

Related to the Technology Insertion issue itself, is the problem facing DoD of how to sustain the military advantages that VHSIC technology will bring. If VHSIC were predominantly useful only for military purposes, the approach to the problem would be reasonably simple. However, VHSIC will not only provide a very advanced technology for military use, but may also have even

broader applicability in commercial and industrial markets. Judging from the recent history of IC development, commercial applications will ultimately dominate the market for VHSIC technology. However, while VHSIC is being developed and as long as the major needs and uses of VHSIC lie in the military arena, the decision has been made at the Secretary of Defense level to protect the military advantages offered by the VHSIC technology and its applications through adequate security measures. The form of these measures and the actions to be taken to execute them are now being developed.

II IMPACT OF THE INSERTION OF VHSIC TECHNOLOGY ON SYSTEM LEVEL RELIABILITY/AVAILABILITY

A. INTRODUCTION

The VHSIC program has emphasized the coupling of integrated circuit technology to complex system development and implementation. Foremost among the goals of this program is to significantly increase the mean-time-between-failures for systems utilizing VHSIC technology when compared to a more conventional non-VHSIC implementation. Not only does this increase the probability of a successful mission but it can contribute to lowering the hardware life cycle costs.

This report will indicate the potential impact of VHSIC technology insertion in the areas of both increased reliability and availability. A generalized view and discussion of the potential impact on life cycle costs will be provided.

B. GENERAL DISCUSSION

Many factors affect reliability and modeling the potential reliability of LSI/VLSI circuits becomes extremely complicated. Complete reliability modeling for systems involving these circuits is beyond the capabilities of computers available today. One microcircuit reliability prediction model (Ref. 1) has the general format

$$\lambda p = \Pi_Q \Pi_L \left\{ C_1 \Pi_V \Pi \rho_T + (C_2 + C_3) \Pi_E \right\}$$

where

λp is device failure rate in F/10^6 hour

Π_Q is device quality factor

Π_L is learning factor

Π_V is voltage derating stress factor (CMOS devices only)
$\Pi_{\rho T}$ is ROM and PROM programming technique factor
Π_E is application environment factor
C_1, C_2 is device complexity factor
C_3 is package complexity factor

The authors of the referenced paper tested this model against actual failure rate data for a variety of circuits, with the results being quite good. An examination of this paper emphasizes the complexity of developing reliability models for IC circuits. The VHSIC development program represents a tremendous challenge from a reliability modeling point of view since it has attempted to cover a variety of technologies, design approaches, design tools, interconnection schemes, packaging techniques and built-in-test/fault tolerant approaches. Figure 2 gives a summary of some of these implementation approaches. Each of these approaches has the potential to effect the reliability. To further complicate matters, the built-in-test techniques and fault tolerant approaches can significantly improve maintainability, but will alter the reliability of the device.

In spite of the difficulties in developing a realistic model, the impact of VHSIC on both system reliability and maintainability as well as the life cycle costs is anticipated to be considerable. All of the VHSIC vendors expect significant improvement, but few have specific data that allows them to document the impact of applying VHSIC technology.

Several of the vendors are projecting VHSIC chip level failure rates based on extrapolations from their existing data or from the application of MIL STD 217B. These projected failure rates derived from Ref. 2, 3, and 4 are shown in Fig. 3.

Contractor	Technology	Design Approach	Design Tools	Inter-Connection Scheme	Packaging Technique	BIT/FT Approach
Honeywell (Air Force)	Bipolar ISL, CML	Custom-chip Based macrocell library	DAS (Unified Data Base) AIDA (Advanced integrated design automation	Multiplier high speed lead bus & medium speed global bus	Multilayer ceramic carrier with beantape inter-connections	LSSD signature analysis
Hughes (Army)	CMOS on SOS	Standard and custom recon-figurable chips	Hercules CAD data base	pipeline interconnects	leaded ceramic flatpack leads on 25 mil pitch	set/scan, signature analysis redundancy
IBM (Navy)	NMOS	Master image with microcell library	VHD^{2}L (VHSIC Hard-ware design and description language) EDS engineering design system	pipeline on chip	single chip flexible film module package	LSSD, signature analysis, redundnacy parity
Texas Instruments (Army)	Bipolar STL, NMOS	Programmable chip set	HDL, INTSIM (integrated simulator)	Multi-master synchronous paralles bus (S-bus)	JEDEC Type C leadless chip carrier	error correcting code, TMR
TRW/ Motorola (Navy)	Bipolar 3d TTL CMOS	Standard chip set	ADLIB/SABLE HSL-Hierarchical Systems Language multilevel data base	V-bus inter-connect (multiloop)	Ceramic Hermetic chip carrier, 132 edge chip attach	Set/Scan
Westinghouse	Bluk CMOS	Standard chip set	ISPS, LOGIC V, ASSIST, CABBAGE CALMA	Dual phase open drain bus and high speed ring network	leaded chip carrier with 25 mil pitch	RADSS (Scan/ set)

FIGURE 2. VHSIC Phase I Reliability - Related Approaches

VENDOR	Number of Chip Types	Chip Complexity (in equiv. gates)	Anticipated Chip Failure Rate (Failures/hour)
Westinghouse	6	5,000 to 31,000	19.4×10^{-6}
IBM	1	38,000	3×10^{-6} $.3 \times 10^{-6}$ ('84) $.3 \times 10^{-6}$ ('87) 6×10^{-8} ('89)
Hughes	3	Based on a 300 gate CMOS/SOS chip operating at room temperature	6.92×10^{-12}
VHSIC GOAL	-	-	6×10^{-8}

FIGURE 3. Failure Rates

Note that the VHSIC goal is 6×10^{-8} failures per hour. The Hughes failure rate can probably be discounted because of the vehicle used (a 300 gate-gate array) to determine the failure rate. IBM is anticipating meeting the VHSIC goal of 6×10^{-8} failures per hour when the device is in limited production about 1988. The calculations used in the subsequent sections of this report assume three values for the VHSIC failure rate; the first is the Westinghouse figure of 20×10^{-6} failures per hour, the second is 10^{-6} failures per hour, and the third is the VHSIC goal of 6×10^{-8} failures per hour.

There are two components to the availability equation; reliability and maintainability. The equation can be simply expressed as follows:

$$\text{Availability} = A(t) = 1 - \frac{MTTR}{MTBF}$$

where, MTTR is the mean-time-to-repair

and MTBF is the mean-time-between-failure

Based on the above equation, if the MTTR goes to zero the availability goes to one, regardless of the MTBF. This makes the case for a redundant system, in that while the MTBF is a finite value when a failure does occur, the MTTR effectively is zero. Figure 4 shows the dependence of availability on both the MTTR value and the MTBF. The figure emphasizes the importance of minimizing the MTTR. The change, or delta, in availability when comparing an MTTR of 2 hours to an MTTR of 16 hours is over a factor of eight across an MTBF range of 500 to 2000 hours. This places a heavy emphasis on the requirement for board level and system level tests that ensure the process of recovering from a system failure is as rapid as possible. This means that diagnostics be applied that determine which of the field replaceable units (FRU) has failed. Once the faulty FRU has been replaced (which should be no more complicated that a board removal with a subsequent insertion of the new board), a new set of diagnostics must be run to verify the correct system operation. The use of an in-system diagnostic processor is probably mandatory to ensure the MTTR is minimized.

Figure 5 illustrates the impact on availability resulting from the number of field replaceable units. Note that a relatively high availability (.946) for a unit with an MTBF of 300 hours and an MTTR of 16 hours yields an availability of only .33 when 20 field replaceable units are contained in the system. Note also the importance of a reduced MTTR, since a system with a MTBF of 300 hours and a MTTR of 2 hours yields a higher availability than a system with an MTBF of 2000 hours and a MTTR of 16 hours. Figure 5 emphasizes the heavy dependency availability has on both the MTBF and the MTTR.

There are many missions, however, where the effective MTTR is extended because the repair can not be performed until the mission is completed. In this situation, the critical parameter is the MTBF. Figure 6 shows two sets of curves for the

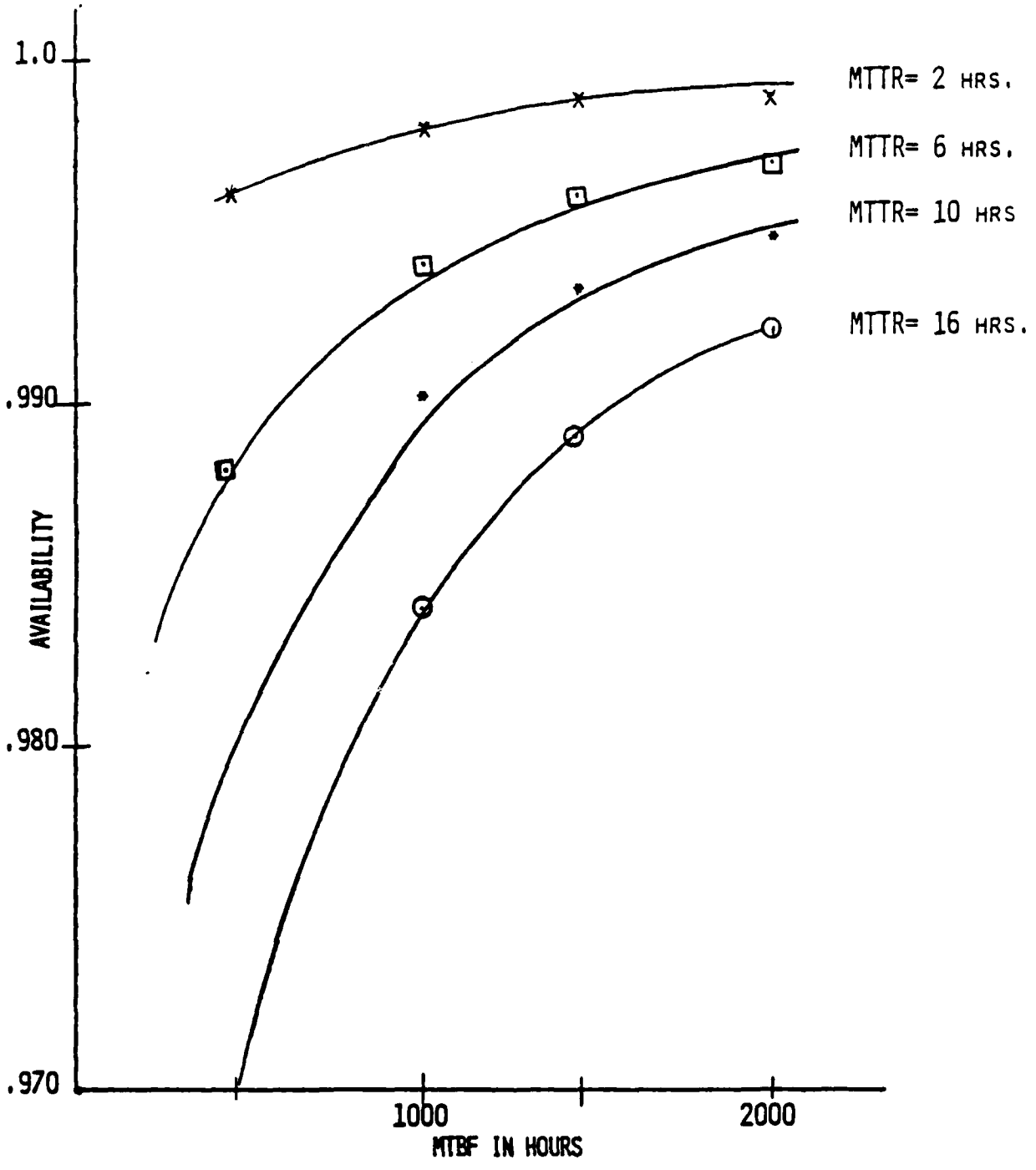


FIGURE 4. Availability Versus MTBF as a Function of MTTR

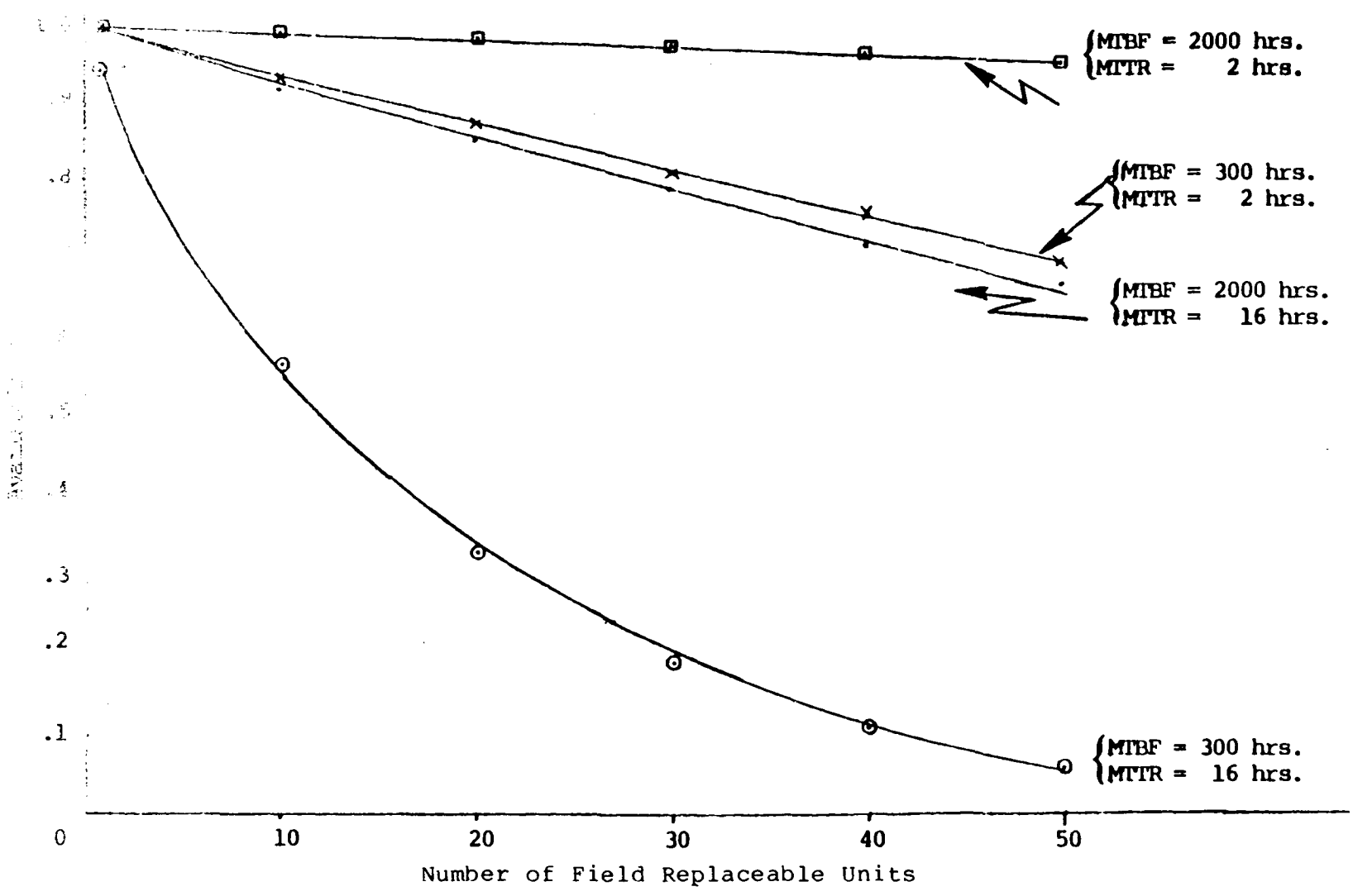
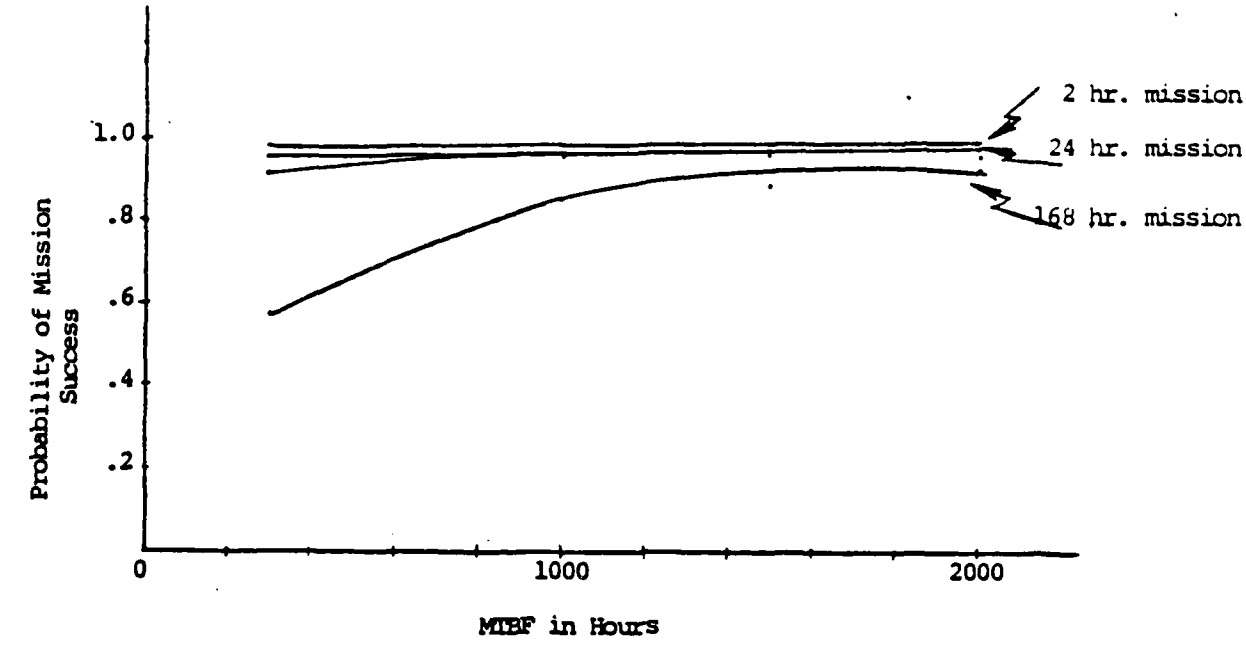


FIGURE 5. Availability Versus Number of Field Replaceable Units as a Function of MTTR/MTBF



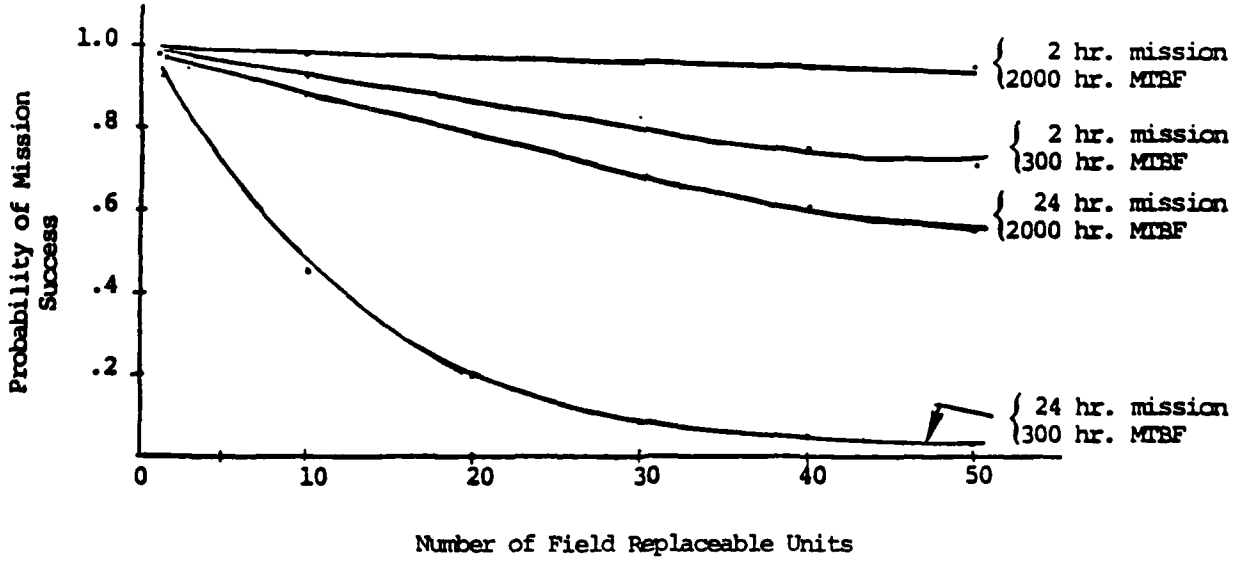


FIGURE 6. Probability of Mission Success Curves

probability of mission success. This is based on a constant hazard model (e^{-t}) and assumes a serial reliability configuration. Again, note the strong dependency of mission success on the number of field replaceable units contained in the system.

Indirect savings from the application of VLSI can provide significant benefits; specifically, it allows the size, weight and power requirements to be significantly reduced in most electronic based systems. Data indicated that in avionics applications, IC's account for approximately 2 percent of the avionic failures and only 1 percent of the total aircraft failures (Ref. 5). The same data indicates that such items as cabling and maintenance operations contribute approximately 85 percent of the total avionics failures. Use of the VHSIC chips can significantly reduce the support hardware (like cables) as well as providing for a self-test concept that will minimize failures that occur as a result of the maintenance approach. When VHSIC technology is applied, emphasis should be placed on redesigning both the logic implementation and the packaging to maximize the advantages of the VHSIC insertion. A "pin-for-pin" replacement of existing SSI/MSI/LSI parts with VHSIC equivalents will reduce the total IC part count but will not significantly reduce the packaging necessary to support this type of system implementation.

C. EXAMPLES

1. Specific Manufactures Examples

All six Phase 1 contractors were contacted regarding the availability of both VHSIC chip reliability data and information regarding the impact of VHSIC technology insertion on equipment "life cycle costs." Several of the manufacturers were willing to quote projected reliability figures. As indicated in the previous paragraphs, these figures converged to the VHSIC reliability goal of 6×10^{-8} failures per hours.

Westinghouse had some preliminary information regarding the insertion of VHSIC technology in an F-16 radar computer (Ref. 6.) The data shown in Fig. 7 is compiled from the Westinghouse information and is based on the following three implementation scenarios:

(1) An insertion of VHSIC chips (in this case, 8000 gate-gate arrays) into a logic configuration with the number of boards remaining constant, as compared to the baseline configuration, but with the total chip count being substantially reduced.

(2) An insertion of the same VHSIC 8000 gate-gate into a logic implementation that was reconfigured to maximize the use of the gate arrays while at the same time reducing the total board compliment.

(3) An insertion of high density VHSIC chips (with an average per chip gate complexity of approximately 27,000 gates) into a logic implementation that was reconfigured to maximize the use of these high density chips and designed to minimize the board count. Some VHSIC gate arrays are included in this design.

It must be emphasized that the first two implementation scenarios use gate array chips, while the third scenario used both gate arrays and the higher density custom/semi-custom VLSI chips. Some of the specific information obtained from Westinghouse is summarized in Fig. 7.

Configuration	SSI/MSI/LSI IC Pack. Ct.	VHSIC Pack. Ct.	VHSIC Gate Array Pack. Ct.	Performance	MTBF
Baseline	6,000	--	--	X	330
Scenario (1)	895	--	55	X	756
Scenario (2)	917	--	33	1.25xto2.3x	1311
Scenario (3)	600	yes *	5	2.8xto3.0x	2067

FIGURE 7 VHSIC Chip Insertion

*Number of high-density
Type VHSIC chip used was not defined

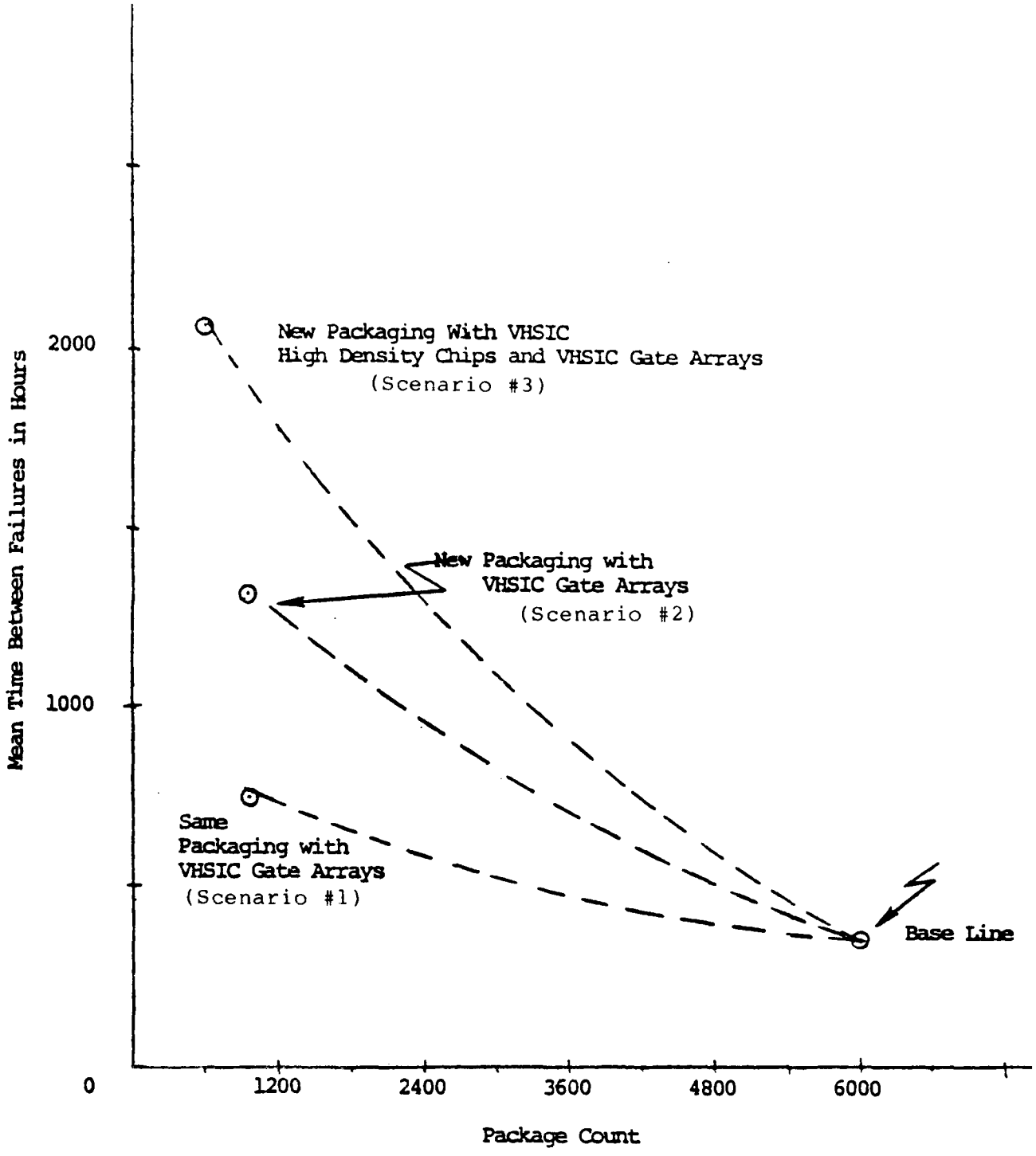


FIGURE 8. MTBF Versus Packaging for Westinghouse Data

Figure 8 shows the MTBF as a function of the package count for the "baseline" Westinghouse configuration and the three scenarios detailed above. Note the significant impact on MTBF when new packaging is used (the difference between scenario 1 and 2) yields almost a factor of two increase in MTBF. Additionally, from the previous chart and Fig. 8, not only does the MTBF increase as a result of the VHSIC insertion, but the performance increases up to a factor of 3.

It is apparent from this data that the system reliability is considerably enhanced when VHSIC technology is applied. Figure 9 projects the impact of this technology on both acquisition costs and field support costs. Again, this data was obtained from Westinghouse:

Configuration	Total Package Count	Performance	Acquisition Cost	Field Support Cost
Baseline	6,000	X	X	X
Scenario (1)	950	X	X	.43X
Scenario (2)	950	1.25xto2.3x	.6X	.2X
Scenario (3)	600	2.8xto3.0x	.33X	.1X

FIGURE 9. VHSIC Insertion Costs

VHSIC technology insertion demonstrates up to a factor of three reduction in the purchase price and up to a factor of 10 reduction in field support cost. Note that the significant reduction in field support cost is partially attributable to reducing the number of maintenance stages from three to two.

2. Potential Effects of VHSIC Insertion on System Implementation

Since many of the vendors were not able to provide hard data on both the failure rate numbers and the impact of VHSIC insertion on life cycle costs, we can postulate as to the potential benefits.

The following paragraphs discuss several possible implementation scenarios and detail the the impact of VHSIC insertion on the reliability of these hypothetical systems. Figure 11 is a summary of VHSIC chips and their approximate gate complexity from the six Phase 1 vendors. There are two comments to be made regarding the numbers in Fig. 11. The first comment is that the determination of the number of equivalent gates is at best a good estimate, with each vendor having their own algorithm for this estimation. In addition, many of the chip designs are still in a state of flux and final determination of both the number of devices and the number of equivalent gates is not possible.

Nonetheless, we can generate, based on the numbers in Fig. 11, an estimated gate complexity for a VHSIC chip. This number calculated to be approximately 16,000 gates if the gate array chips are included, and approximately 20,000 equivalent gates without the gate array chips.

The effect of the "average" VHSIC chip on a system implementation can be calculated by assuming a percentage of the total system is integrated into the VHSIC chips. For Figs. 12 and 13, a hypothetical system implementation of 200,000 gates, 300,000 gates and 400,000 gates was chosen. The MTBF was calculated for a baseline system implementation using SSI/MSI/LSI parts that yielded an average of 60 gates per integrated circuit package. A wide range of failure rates are available for these parts (7, 8); the assumed failure rates and the distribution of the usage of SSI versus MSI versus LSI is summarized in Fig. 10.

Type	% of Utilization	Assumed Failure Rate(f/hr)
SSI	45	3×10^{-9}
MSI	45	30×10^{-9}
LSI	10	300×10^{-9}

FIGURE 10. Parts Failure Rate

These numbers yielded a composite failure rate of 45×10^{-9} failures per hour.

Chip Type	Manufacturer	# of Devices	# of Equiv. Gates	# of I/O's	Comment
P^3	Honeywell	117,000	11,500	160	10k bits of RAM
I/O CRTL	"	79,000	12,500	N/A	
I/O CRTL	"	54,000	11,000	N/A	
CORREL.	Hughes	97,300	24,300	124	
S^3	"	66,000	16,500	104	
ABD	"	59,700	14,900	25	
CMAC	IBM	N/A	37,000	184	
GBU	TI	TBD	4,000	68	Gate Array
DPU	TI	TBD	10,000	84	Gate Array, with 52K ROM
DIU	"	TBD	10,000	84	" " " "
ACS	"	TBD	10,000	68	" " " "
VAG	"	TBD	10,000	68	" " " "
VALU	"	TBD	14,300	84	Includes 96K of ROM
SRAM	"	TBD	N/A	32	8Kx9 SRAM
MS-MPS	TI	TBD	4,000	108	Gate Array
WAM	TRW	48,000	16,000	113	
CAM	"	48,000	17,000	116	
[illegible]	"	90,000	N/A	94	
AG	"	TBD	13,000	62	
[illegible]	Westinghouse	112,000	28,000	196	
ALU	"	90,000	22,500	196	
FXP-ALU	"	124,000	31,000	196	
[illegible]	"	120,000	30,000	204	
[illegible]RAM	"	400,000	N/A	52	
G.A.	"	20,000	5,000	120	Gate Array

FIGURE 11. Parameter Summary of VHSIC Chips

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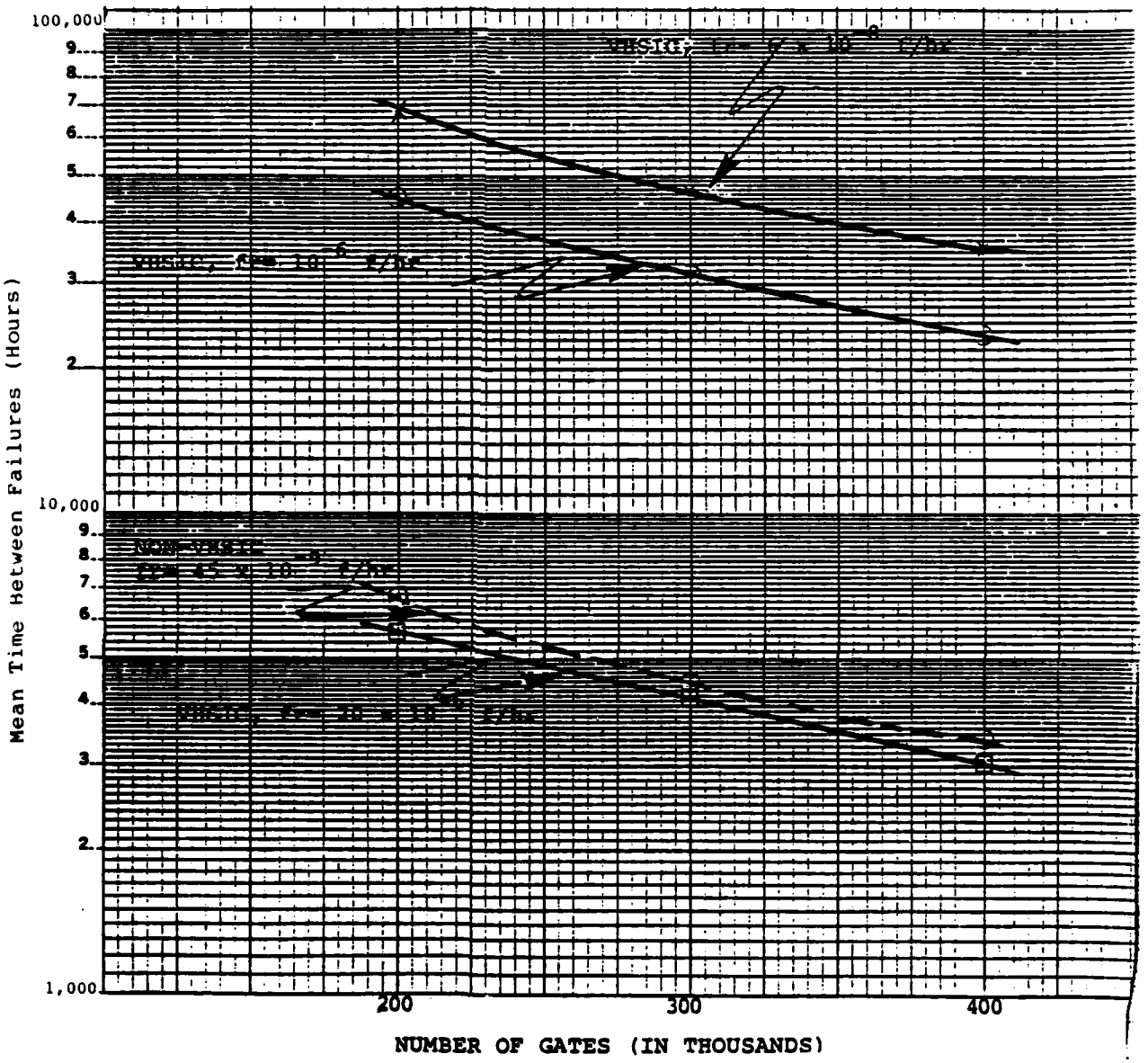

FIGURE 12. MTBF Versus Number of Gates with 25% of Gates in SSI/MSI/LSI

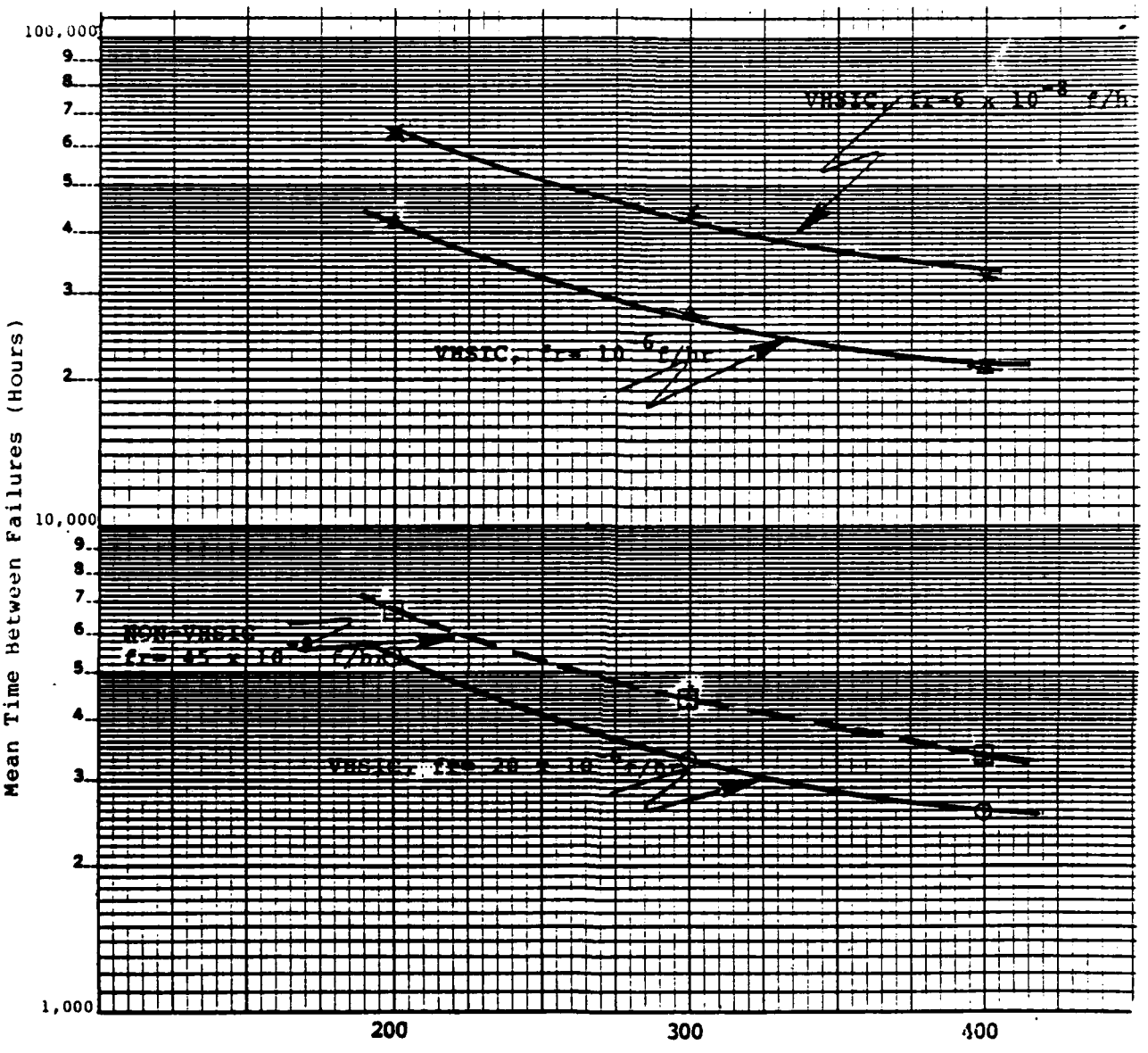

FIGURE 13. MTBF Versus Number of Gates with 10% of Gates in SSI/MSI/LSI

A VHSIC based MTBF was then calculated based on three failure rates, the first being the Westinghouse projected figures of $20x10^{-6}$ failures per hour, the second is 10^{-6} failures per hour, and the third is the VHSIC goal of $6x10^{-8}$ failures per hour. Note that this is greater than a factor of 300 in the spread of failure rate numbers. To calculate the projected VHSIC based system level MTBFs, the following assumptions were made:

1. The non-VHSIC (SSI, MSI, LSI) failure rate is approximately $17x10^{-9}$ failures per hour. It is assumed that a large percentage of the LSI components become a part of the VHSIC chips.

2. Figure 10 assumes 25 percent of the logic remains in SSI, MSI, and LSI.

3. Figure 11 assumes 10 percent of the logic remains in SSI, MSI, and LSI.

4. All memory intensive components are separate.

5. The non-VHSIC integrated circuit average gate density per package is 60.

6. The "average" VHSIC integrated circuit gate density per package was 20,000.

The results of these calculations are shown in Fig. 12 and Fig. 13. Note in both of these figures the advantage of using VHSIC technology when the failure rate is less than $20x10^{-6}$ failures per hour. Using this higher number generates an MTBF which is lower that the SSI/MSI/LSI implemented system, although this high failure rate does yield a system MTBF close to those of the non-VHSIC

implemented system. What must be emphasized is these calculations do not include the potential benefits to the system level MTBF by the reduction in the board count, cable requirements, connectors, etc. If calculations were to be performed detailing all the system level components of the VHSIC implemented system, even with a component level failure rate of 20×10^{-6} failures per hour, it would show a substantial improvement in MTBF compared to the non-VHSIC system.

D. CONCLUSIONS

The following items summarize our conclusions regarding the impact on system level reliability/availability resulting from the application of VHSIC technology:

1. Although specific system level implementation studies were limited to one contractor, the data obtained from this study showed a range in the MTBF improvement from factors of 2.3 to 6.2 and an increase in system level performance that ranged from a factor of 1.25 to a factor of 3.0. In addition, life cycle costs were significantly impacted by a factor of 3 reduction in acquisition cost and up to a factor of 10 decrease in field support cost.

2. The study of the VHSIC technology insertion on the hypothetical system continuing up to 400,000 gates, yielded system level MTBFs that were, at worst, comparable to an identical system implementation using SSI/MSI/LSI components. If the VHSIC goal of 6×10^{-8} failures per hour is achieved, then very significant (a factor of 10 at the component level) increases

in MTBF will be obtained. In addition, insertion of VHSIC technology should substantially reduce system level failures through the reduction of system support components such as cables, connectors, printed circuit boards, etc. The combination of the VHSIC failure rate goal of $6x10^{-8}$ and the potential reduction of system support components should yield at least an order of magnitude improvement in MTBF's when compared to the SSI/MSI/LSI implemented system.

3. System level availability is a function of both MTBF and MTTR. At the system level emphasis must be placed on reducing the MTTR to as low a number as possible. The mechanism for recovering from a system failure should include the application of system level diagnostics (through the use of a diagnostic processor), the identification of the failed field replaceable unit (FRU), with the subsequent removable of the failed FRU and insertion of a new FRU. System level diagnostics must then be run to verify system level operation. MTTR should be measured in terms of minutes rather than hours.

4. It is apparent that the vendors are in the very early stages of the system application of these complex integrated circuits. As a result, little specific system implementation information, particularly with regard to life cycle costs, is available from the vendors.

III SUMMARY AND RECOMMENDATIONS

To address the issues associated with VHSIC and to understand the recommendations relative to R&M plans, it is important to appreciate the current and planned activities of the VHSIC program. First of all, VHSIC differs from the other 15 technologies studied in this report (with the exception of Software, e.g., Software Initiative, Ada, etc.) in that a bonafide Program Office exists, that several of the issues pertinent to the overall objective of this study are being addressed, and that the mechanism for new studies, demonstrations, and developments pointed specifically to R&M issues is in place when funding becomes available.

It has been stated that the United States leads the world in under-utilization of its available technology (with Great Britain a distant second). Be that as it may, and for whatever reason(s), the time lag between development of a technology and its application to military systems is deemed unacceptable. Recognizing this, the VHSIC Program Office has initiated several activities. The first is a Yield Enhancement Program, designed to rapidly move VHSIC components from the prototyping stage to the high volume, low cost requirements of both peacetime and wartime environments and to ensure component availability whatever the environment. A second program is the VHSIC Insertion Program, designed to identify and resolve issues which define barriers to the early-on utilization of VHSIC technology. As a part of the Insertion Program studies, it was determined that automated design tools was one of the keys to expediting VHSIC technology into real world systems. To this end, a separate and supporting activity, the Integrated Design Automation System (IDAS) program was initiated. This effort is in the planning stage, chaired by the VHSIC Program Office with tri-Service representation on the steering committee, and is supported by the Institute for Defense Analyses, other consultants from the private sector and university faculties.

This planning by the IDAS committee consists of the following activities: (1) a survey of industry, government laboratories, and universities for tools and techniques pertinent to IDAS; (2) definition of both long and short term road maps for the development of IDAS; and (3) definition of a hierarchical methodology and language for the top-down definition, design and documentation of systems (by default, named SDL). It is important the SDL provide the methodology and description from the system level for the following reasons. First, the boundaries between analog and digital implementation are constantly moving, in favor of digital, as higher performance A/D converters and VHSIC technologies come on line. Secondly, even for those portions of the system which remain analog, the analysis of BITE and fault-isolation data and the system control (reconfiguration, mode change, etc.) will most likely be done digitally. Additionally, such a description aids the system designer in the all important decisions of mapping functions to hardware elements (chips, boards, LRU's WRA's etc.) for both fabrication and maintenance ease.

As should be obvious, the *VHSIC program* tends to overlap several of the other technologies studied in this report. For example, Artificial Intelligence (as applied to CAD/CAM), and CAD/CAM itself (e.g., the recently awarded VHSIC Hardware Description Language [VHDL])with its supporting analysis and simulation tools. On the software side, the SDL methodology is intended to provide the requirements, both functional and temporal, at the interface with software implementation languages (in particular, Ada). Likewise, the SDL is planned to interface with VHDL. It is too early to establish packaging and interconnect standards. The problem is not being ignored, however, as exemplified by the recently completed study (PAVE PILLAR, May 1983) sponsored by the Army and the Air Force. This study was particularly directed to interface issues associated with the products of two VHSIC contractors (Texas Instruments and Westinghouse.)

A. R&M INITIATIVES

With all of the above in mind, what is needed by the VHSIC program from an R&M viewpoint? Certainly, every effort is being made by the VHSIC Program Office to ensure the reliability of the VHSIC components themselves. But the "proof of the pudding", so to speak, is the behavior of these components in a system (or subsystem) application. Such a demonstration/test program, pointed specifically to R&M issues, is strongly recommended. While VHSIC components are not yet available, there exist many important factors involved in achieving a successful demonstration/test program. Certainly, the establishment of a feasible schedule and adequate budget is a requirement. There are many technical issues associated with such a program that must be addressed, however. First, the explicit goals of the demo/test (from an R&M viewpoint) must be defined. The types of tests, the environment of the tests, the data to be collected, the analysis required on the data and the specification and procurement (if required) of any ancillary hardware for monitoring and data collection are among these issues. Because of the diversity of the semiconductor technology, applications, and BITE and fault-isolation technologies among the six Phase 1 VHSIC contractors, it is important that a minimum of three systems (subsystems) be subjected to the demo/test program.

As is well-known, such a program is only as good as the "front end" engineering which precedes the actual demo. Recognizing the need for such engineering, the normal delays in vendor selection and contract awards, it is deemed essential that the recommended program be initiated as soon as funds are available so that it is in place to support the continued maturation of this most important and promising technology, without untimely delays.

In addition to the forementioned R&M demonstrations, which could be accomplished using VHSIC Phase 1 brassboard systems, the following recommendationms are also given:

1. Requirements Review.

Direct the early planning for VHSIC technology demonstration and insertion through incorporation of VHSIC requirements in the DSARC and the Service's System Acquisition Review Council (SSARC) for the signal and data processing portions of systems entering development in or after FY84 and production after FY86. VHSIC planning in appropriate system R&D programs exceeding $10M and system production programs exceeding $100M should be required. An R&M committee should produce a list of systems for which this would apply.

2. Availability Studies.

VHSIC technology has the ability to offer greater subsystem A_i due to built-in-test and potential for fault-tolerant designs. An examination of current operational systems should be performed to establish system level A_i data based on the use of VHSIC. This study could be effectively performed by mapping VHSIC technology onto the existing system level R&M case studies.

The Defense Science Board Summer Study on Operational Readiness with High Performance Systems stated that "the maintenance concepts for high performance systems have been force fit into maintenance and repair structures which are often not well matched to today's systems." One should design such a structure in the light of technology and performance of modern systems. The VHSIC technology has the potential to increase A_o by impacting the cost of operational system field support and the possible elimination of a level of maintenance. It is recommended that a study be performed to quantify the impact of VHSIC on A_o. It should give due regard to factors such as personnel, training, spares, survivability, transportation, response time, etc., and develop alternatives to the current maintenance concepts for high performance systems. This study should be performed as part of the VHSIC Technology Insertion Program.

3. R&M Recommendation.

It is recommended that adequate VHSIC reliability should be demonstrated before actual insertion in operational systems. The integrated circuit A_i will be demonstrated in the VHSIC program. In addition, a reliability and maintenance demonstration at the system level should be developed as part of the VHSIC Technology Insertion Program.

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